Amendments to the Specification:

Please replace the title on page 1, lines 1 and 2 "**ARCHITECTURES FOR A MODULARIZED DATA OPTIMIZATION ENGINE AND METHODS THEREFOR**" with the title "ARCHITECTURES FOR A MODULARIZED DATA OPTIMIZATION ENGINE AND METHODS THEREFOR"

Please replace the heading on page 1, line 4 "**BACKGROUND OF THE INVENTION**" with the heading "BACKGROUND OF THE INVENTION"

Please replace the heading on page 11, line 1 "**SUMMARY OF THE INVENTION**" with the heading "SUMMARY OF THE INVENTION"

Please replace the heading on page 12, line 1 "**BRIEF DESCRIPTION OF THE DRAWINGS**" with the heading "BRIEF DESCRIPTION OF THE DRAWINGS"

Please replace the heading on page 15. line 1 "**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**" with the heading "DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS"

Please replace the title on page 114, lines 1 and 2 "**ARCHITECTURES FOR A MODULARIZED DATA OPTIMIZATION ENGINE AND METHODS THEREFOR**" with the title "ARCHITECTURES FOR A MODULARIZED DATA OPTIMIZATION ENGINE AND METHODS THEREFOR"

Please replace the paragraph starting on page 5, line 7 with the following paragraph.

The same three issues pertaining to main memory 106 (i.e., the speed of data transfer to and from memory, the operating speed of the memory, and the storage capacity) also apply to Network-Assisted Storage (NAS) systems, storage area networks (SANs), RAID storage

systems, and other networked electromagnetic or optical-based data storage systems. With reference to the arrangement 200 in Fig. 2, irrespective of the protocol implemented on a transmission link 202 between a drive controller 204 and the actual storage media 206 (e.g., hard disks, optical platters, and the like), storage performance can be improved if the effective data throughput through transmission link 202 can be improved. This is true irrespective whether the protocol implemented is serial ATA (S-ATA), IDE, FCAL, SCSI, Fiber Channel over Ethernet, SCSI over Ethernet, or any other protocol employed to transfer data between disk controller 204 and storage media 206. With respect to the storage capacity issue, there is a fixed capacity to storage media 206 based on physical limitations and/or formatting limitations. From a cost-effectiveness standpoint, it would be desirable to transparently increase the capacity of storage media 306 without requiring a greater number and/or larger platters, or changing to some exotic storage media.

Please replace the paragraph starting on page 46, line 19 with the following paragraph.

Also in row R11, the value 4 was noted to have been associated with CAM address location 11 earlier (see row R2) [[(Fig. 12: 1226/1216)]] (Fig. 12: 1226/1215). In one advantageous embodiment, a small shadow memory, which is employed to store associative pairings between a CAM content value and its associated CAM address, is searched to determine which CAM address was used previously to store the value 4 (Fig. 12: 1228). That is, the shadow memory addresses are the counter values, and the content stored at each address in the shadow memory is the CAM address currently used to store the counter value that forms the shadow memory address. The use of a shadow memory advantageously allows the CAM address to be rapidly ascertained for any given counter value. This shadow memory is updated every time there is an update to the CAM. Once this CAM address location 11 is ascertained, it is freed up in the CAM (Fig. 12: 1230). In other words, CAM address 11 is now considered free to store another value. In one embodiment, each CAM address has associated with it a Free/Not Free flag bit, and the flag bit is set whenever that CAM address is written to and reset when that CAM address is freed. Alternatively or additionally, the content of that CAM address may be

reset to 0 when the CAM address is freed. Once CAM address location 11 is freed, the value 4 is written into location 61 (Fig. 12: 1216), and the code value 6 is outputted (Fig. 12: 1218/1220/1204).

Please replace the paragraph starting on page 50, line 8 with the following paragraph.

Also in row R17, the value 4 was noted to have been associated with CAM address location 61 earlier (see row R11) [[(Fig. 12: 1216)]] (Fig. 12: 1215). Once this CAM address location 61 is ascertained (Fig. 12: 1228), it is freed up in the CAM (Fig. 12: 1230). In other words, CAM address 61 is now considered free to store another value. Once CAM address location 61 is freed, the value 4 is written into location 10 (Fig. 12: 1216), and the code value 1p is outputted (Fig. 12: 1218/1220/1204).

Please replace the paragraph starting on page 50, line 14 with the following paragraph.

In row R18, the input character is 1r (Fig. 12: 1206). Now the bit pattern is 0q1r (Fig. 12: 1208), which is a merging of what remains (0q) of the previous bit pattern for searching (1p0q) after a code is outputted (1p). Since 01 is not in the dictionary [[(Fig. 12: 1216)]] (Fig. 12: 1210), the counter value is increased to 5 (Fig. 12: 1212/1214) and is written to the CAM at CAM address 01 (Fig. 12: 1216). The output code is 0q (Fig. 12: 1218/1220/1204).

Please replace the paragraph starting on page 51, line 3 with the following paragraph.

In row R20, the input character is 1t (Fig. 12: 1206). Now the bit pattern is 61t (Fig. 12: 1208), which is a merging of the content of CAM address location 11 (which is 6 as shown in row R16), and the new input character 1t. Since CAM address 61 is not used in the dictionary (it was freed up in row R17), the counter value is increased to 6 (Fig. 12: 1210/1212/1214). In row R20, the value 6 was noted to have been associated with CAM address location 11 earlier (see row R16) [[(Fig. 12: 1216)]] (Fig. 12: 1215). Once this CAM address location 11 is ascertained (Fig. 12: 1228), it is freed up in the CAM (Fig. 12: 1230). In other words, CAM address 11 is

now considered free to store another value. Once the CAM address 11 is freed, the counter value is written to the CAM at CAM address 61 (Fig. 12: 1216). The output code is 6 (Fig. 12: 1218/1220/1204).